REMARKS

This Response responds to the Office Action dated September 30, 2004 in which the Examiner objected to the drawings, rejected claims 1, 7-9, 15 and 21-23 under 35 U.S.C. §102(b) and objected to claims 2-6, 10-14, 16-20 and 24-28 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

Attached to this Response is a replacement sheet in order to label Figures 1 and 2 prior art. Applicants respectfully request the Examiner approves the correction and withdraws the objection to the drawings.

Claim 1 claims an integrated circuit comprising a biasing circuit for maintaining the transconductance of a Gm cell constant and claim 15 claims a method of maintaining the transconductance of a Gm cell on an integrated circuit constant. The integrated circuit comprises an on-chip constant voltage source and an on-chip constant current source. The on-chip constant current source has a connection for an external resistance. The value of the external resistance determines the current generated by the constant current source. The biasing circuit and method comprises providing a first fraction of the current generated by the on-chip current source to bias the output of the Gm cell. Next, a second fraction of the voltage generated by the on-chip voltage source is provided for biasing the input of the Gm cell. The transconductance of the Gm cell is controlled to be equal to a ratio of a fraction of the current generated by the on-chip current source to the fraction of the voltage generated by the on-chip voltage source.

Through the structure and method of the claimed invention a) controlling the transconductance of a Gm cell and b) controlling the transconductance to be equal

to a ratio of a fraction of a current generated by an on-chip current source to a fraction of a voltage generated by an on-chip voltage source as claimed in claims 1 and 15, the claimed invention provides an integrated circuit and method of maintaining the transconductance of a cell constant without requiring the use of an external frequency reference, an external resistor or any extra external pins. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 15.

Claims 1, 7-9, 15 and 21-23 were rejected under 35 U.S.C. §102(b) as being anticipated by *Iga* (U.S. Patent No. 6,124,738).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(b). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Iga appears to disclose an input buffer for a semiconductor device and, more particularly, an input buffer for a semiconductor device receiving an external reference potential and an external signal obtained by superposing a logic signal of a small amplitude on the external reference potential, comparing the external reference potential with the external signal and applying an internal signal corresponding to the result of comparison to an internal circuitry. As the speed of operation of microprocessors has been increased recently, speed of operation of a memory has also been increased. As to data transfer between devices, however, the speed of operation is limited when the conventional TTL (Transistor Transistor Logic) based interface is used. TTL based interface does not present any problem as along as the operational frequency is low. However, when the operational frequency is

made higher, an overshoot or an undershoot of an output signal is noticed and, in addition, in a bus transmission system, irregularity of signals caused by reflection has come to be a serious problem. In view of the foregoing, a high speed interface in which signal amplitude is made smaller, has come to be practically used. (col. 1, lines 8-29) Therefore, an input buffer is provided for a semiconductor device which operates normally even when an arbitrary potential between first and second potentials is applied as an external reference potential. Briefly stated, a potential converting circuit converts an external reference potential to a predetermined potential, a signal converting circuit converts an external signal to a signal obtained by superposing a complementary signal of a logic signal with small amplitude on a predetermined potential, a comparing circuit compares an output potential of the potential converting circuit with an output signal of the signal converting circuit, and outputs an internal signal based on the result of comparison. Therefore, even when an arbitrary potential between first and second potentials is applied as an external reference potential, normal operation is ensured. (col. 3,line 55 through col. 4, line 4)

Thus, *Iga* merely discloses a high speed interface in which signal amplitude is made smaller to avoid an overshoot or undershoot during signal transmission. Nothing in *Iga* shows, teaches or suggests controlling transconductance of a Gm cell as claimed in claims 1 and 15. Rather, *Iga* merely discloses a high speed data transfer system in which signal amplitudes are made smaller.

Additionally, *Iga* merely discloses a) a converting circuit that converts an external reference potential to a predetermined potential, b) a signal converting circuit which converts an external signal to a signal obtained by superimposing a

complementary signal of a logic signal with small amplitude on a predetermined potential, c) a comparing circuit which compares the output potential of the potential converting circuit with the output signal of the signal converting circuit and d) outputs an internal signal based on the result of the comparison. Thus, nothing in *Iga* shows, teaches or suggests controlling transconductance to be equal to a ratio of a fraction of a current generated by an on-chip current source to a fraction of a voltage generated by an on-chip voltage source as claimed in claims 1 and 15. Rather, *Iga* merely discloses a potential converting circuit, a signal converting circuit and a comparing circuit.

Since nothing in *Iga* shows, teaches or suggests a) controlling transconductance of a Gm cell and b) controlling the transconductance to be equal to a ratio of a fraction of a current generated by an on-chip current source to a fraction of a voltage generated by an on-chip voltage source as claimed in claims 1 and 15, applicants respectfully request the Examiner withdraws the rejection to claims 1 and 15 under 35 U.S.C. §102(b).

Claims 7-9 and 21-23 depend from claims 1 and 15 and recite additional features. Applicants respectfully submit that claims 7-9 and 21-23 would not have been anticipated by *Iga* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 7-9 and 21-23 under 35 U.S.C. §102(b).

Since objected to claims 2-6, 10-14, 16-20 and 24-28 depend from allowable claims, applicants respectfully request the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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Date: February 28, 2005

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